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Efficient Synthesis of Reversible Circuits Using Quantum Dot Cellular Automata

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ABSTRACT Heat dissipation is one of the major problems in the construction of electronic devices. Reversible computing is one of the emerging computing paradigms to overcome heat dissipation problem. One of the nanoscale devices that has low power consumption and can be used to construct digital logic components is quantum-dot cellular automata (QCA). In this paper, the benefits of reversible computing of QCA will be used to propose QCA designs for two main reversible gates, the CNOT and the TOFFOLI gates. The proposed CNOT gate has been used to design QCA for double CNOT gate to show its reversibility, and QCA design for the SWAP circuit that contains 3 CNOT gates. The suggested TOFFOLI gate is utilized to construct QCA for double TOFFOLI gate and a reversible circuit which consists of several reversible gates. The suggested QCA designs for double CNOT, double TOFFOLI and reversible circuits such as SWAP circuit have been proposed by adding cells with certain clocks to the wires that connects the proposed gates. The proposed QCA designs show better cell count, area used in the construction, number of majority gate, wire crossover, and/or clock cycle delay when compared with relevant designs in literature.

INDEX TERMS Quantum-dot Cellular Automata, Reversible gates, Reversible circuits, Double CNOT gate, Double TOFFOLI gate, SWAP circuit

I. INTRODUCTION

In the development of computation paradigms, data loss is one of the main problems [1]. Reversible computation can be used to solve the data loss problem. This can be done by mapping the inputs to unique outputs using a one-to-one and onto mapping (bijection) [1]. Performing reversible computation needs a lot of efforts to explore the capabilities of this emerging technology. A quantum-dot cellular automaton (QCA) is nano-electronics technology which can be used to build reversible circuits [2] [3]. During the last decades, development and investigation in the field of electronic devices made it possible for designers to decrease the size and the power dissipation, and to increase the speed of the components. QCA depends on binary information that is encoded as two free electrons inside the corner of quantum dot cells. There is an interaction between QCA cells due to coulombic interaction that produces computational power. There is no external source delivered to individual internal cells and no current flow between cells [4]. The local interconnections between cells are given by the interaction of cell-to-cell physics because of the order of electron positions [5] [6]. In 1993, Tougaw and Lent presented the fundamental definitions of QCA as arrays of

quantum-dot cells [3] [7]. A unique feature in QCA is a cell that represents the logic state. A cell is a unit with a nanoscale capability of encoding data by configuring two electrons. The cells should be precisely adjusted at nanoscales to provide the proper function. This adjustment will lead to circuit correction through testing these devices for misalignment and fabrication errors [8]. QCA has solved the data loss problem in computation, due to the typical property that QCA has, which leads to low power consumption [9-11].

Reversible logic gates [12], or reversible transformations, are operations applied on a register to perform the computation by changing the states of the system from one state to another. The CNOT gate is a basic element in the synthesis of reversible circuits. The TOFFOLI gate is a universal gate for reversible computation that can be used to implement any boolean function [12].

II. RELATED WORK

Implementing reversible function using QCA has gained wide interest in literature. In [13-17] QCA designs for CNOT gate have been presented. In 2019, a proposed QCA design in [13] of CNOT gate contains 58 cells with 1.5 clock cycle delay as shown in Fig1. In 2016, there is a proposed design in [16] for CNOT gate includes 43 cells with 0.75 clock cycle delay. In 2017, a proposed design in [14] for CNOT gate contains 14 cells with 2 clock cycles delay which is the most cell count effective with respect to the other designs. In 2018, a proposed QCA design in [15] for CNOT gate has been proposed with 23 cells and with 0.5 clock cycle delay as shown in Fig2. Another QCA design for CNOT gate has been proposed in [17] which contains 11 cells with 0.5 clock cycle delay.

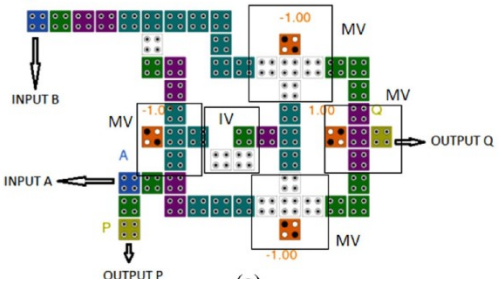


FIGURE 1. ***QCA layout for CNOT gate*** **in [13].**

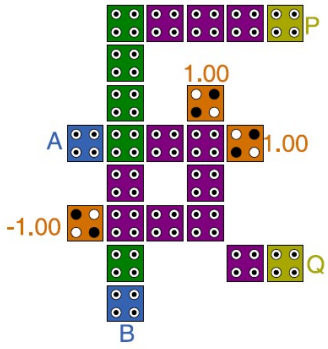
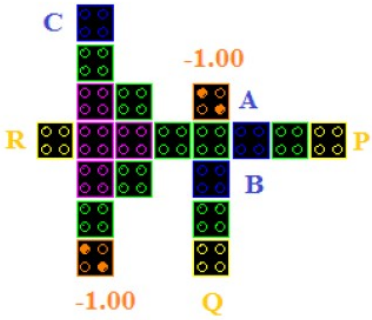


FIGURE 2. **QCA layout for CNOT gate in [15].**



In [15] [18] [19], designs for double CNOT gate have been proposed. In 2014, a proposed QCA design in [18] for double CNOT gate with 51 cells and 0.5 clock cycle delay. In 2015, a proposed QCA design in [19] for double CNOT gate with more cells and cycle delay which is not efficient in comparison with the previous designs, this design contains 93 cells and 0.75 clock cycle delay. In 2018, a proposed QCA design in [15] which contains 40 cells less than the previous design of double CNOT gate and with 0.5 clock cycle delay as shown in Fig3.

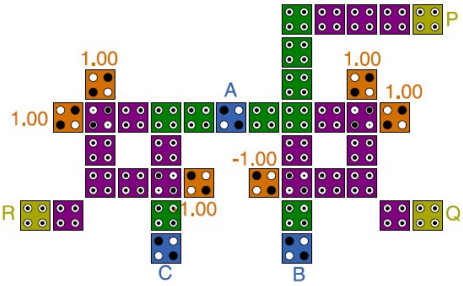


FIGURE 3. **QCA layout for double CNOT gate in [15].**

In [13-15] and [20-22], a lot of designs that used QCA for designing TOFFOLI gate have been presented. In 2019, a design of 64 cells together with 1.5 delay of clock cycle for TOFFOLI gate has been presented in [13] as shown in Fig4. In 2017, there are many designs with less cell count for TOFFOLI gate. A minimized count of cells has been suggested in [20], in which 24 cells are utilized for the construction of the gate with delay of 0.5 clock

cycle. In [21], a multilayer design has been proposed for TOFFOLI gate with 33 cells and 0.75 clock cycle delay. In [22], another design has been proposed for TOFFOLI gate that has the same clock cycle delay as in [21] but it contains 45 cells. In [14], a design has been proposed for TOFFOLI gate with 20 cells but it has 2 clock cycles delay in comparisons with the previous designs as shown in Fig5. In 2018, a proposed QCA design in [15] for TOFFOLI gate with 34 cells and 0.75 clock cycle delay.

FIGURE 4. **QCA layout for Toffoli gate in [13].**

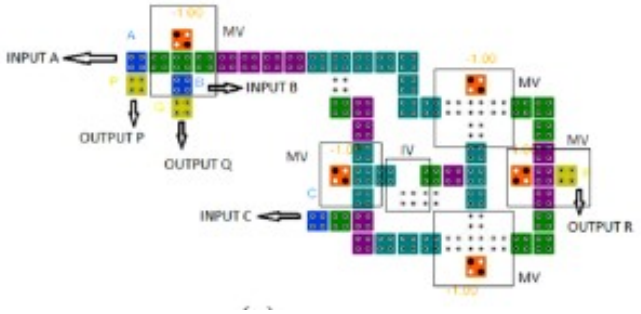


FIGURE 5. **QCA layout for Toffoli gate in [14].**

In [21] [23], designs for SWAP circuit have been proposed. In 2013, a proposed QCA design in [23] for SWAP circuit used 1730 cells and with 9 clock cycles delay. In 2017, a proposed QCA design for SWAP circuit contains 135 cells with clock cycle of 2.75 delays which proved its effectiveness in terms of latency and the number of cells used in the construction compared to designs in previous work as shown in Fig6[21].

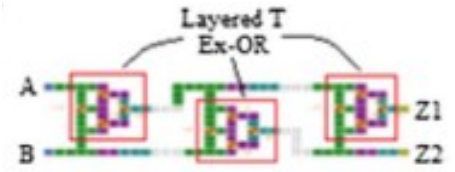


FIGURE 6. **QCA layout for SWAP circuit in [21].**

The problems with previous designs are the increased number of cells used in the construction, number of majority gates, the layers used in the construction, and the clock cycle delay.
The aim of this work is to propose a design of QCA for CNOT gate and TOFFOLI gate. Reversible circuits can be accomplished using reversible gates. Double CNOT and double TOFFOLI gates will be proposed to verify the reversibility of CNOT and TOFFOLI gates. Customization of the proposed reversible QCA makes it possible to implement reversible circuits such as SWAP circuit and circuits that contain combination of reversible gates.
The rest of this paper is outlined in three sections.
Section III gives a review for QCA basic definitions and clocking. Section IV shows the suggested QCA reversible gates and finally, section V concludes the paper.

III. QCA BASICS

Reviewing the main properties of QCA are important before addressing the proposed QCA designs. A review on the physics of QCA cells, basic logic gates, and clocking are given in the next section.

A. BASICS of QUANTUM DOT CONSTRUCTION

QCA cells are used to build the wires of the circuits as well as the computational elements. QCA cell is the main component of QCA device that contains four quantum dots with two mobile electrons positioned in the corners. Allowing an appropriate electrical neighborhood field at the intersections of tunnels will lead the potential boundaries govern the free electrons' movement to supply the separated cell with three status. Invalid cell is the primary status that occurs when the boundaries are decreased by diminishing the electrical field, allowing finding the electrons at any dots. Positive polarization ($P=+1$) is the second status which occurs when the boundaries are increased emphatically. Negative polarization ($P=-1$) is the third status which occurs when the boundaries are increased inversely. The term positive polarization is equivalent to binary logic value '1' and the term of negative polarization is equivalent to binary logic value '0'. The polarization of QCA cell is shown in Fig7 [6].

The QCA cells are set close to one another due to the coulombic interaction between them that allow the cells to be constrained into coordinating polarizations. Equation 1 is the kick energy or the polarization of QCA cell, which is determined by the Columbian interaction between QCA cells, can be measured by electrostatic interaction between all electrons in the two neighbouring cells, *i* and *j* [6]. In [3], more subtle material science elements are presented for the QCA system.

FIGURE 7. QCA cell

$$E^{i,j}=\frac{1}{4\prod \varepsilon_0 \varepsilon_r}\sum_{n=1}^{4}\sum_{m=1}^{4}\frac{qn^i qm^i}{¿rn^i-rm^j\vee¿} \quad (1)$$

Where $\varepsilon_0$is the permittivity of free space, $\varepsilon_r$is the dielectric constant, qn^i is the charge in dot *n* of cell *i* ,$rn^i$is the position of dot *n* in cell *i* and $¿rn^i-rm^j\vee¿$ is the distance between cells.
Equation 2 shows the energy difference between two cells with opposite polarity or with the same polarity can be defined as kink energy [6].

$$Ekink^{n,m}=E^{n,m}{}_{Pn\neq Pm}-E^{n,m}{}_{Pn=Pm} \quad (2)$$

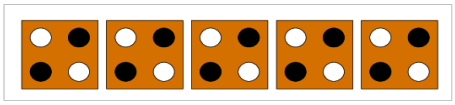
Where *E* is energy *Pn* is the polarization of cell *n* and *Pm* is the polarization of cell m.
Equation 3 can be used to measure the polarization of each cell, according to a recent equation [6].

$$P_i=\frac{\frac{Ekink^{i,j}}{2\gamma}\sum jP_j}{\sqrt{1+¿¿¿}} \quad (3)$$

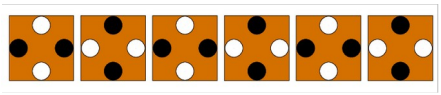
Where P_i is the polarization state of the cell, and P_j is the polarization state of the neighboring cell. γ is the tunneling energy of electrons within the cell.

B. QCA WIRES

The cells of QCA wire give the power to transfer the binary data from input to output due to the coulombic interactions between them. Fig8a presents a QCA wire with 90 degree and Fig8b presents a QCA wire with 45 degree where the polarizations in 45 degree wire interchanges of binary signals between the *+1* and *-1* polarizations [24].



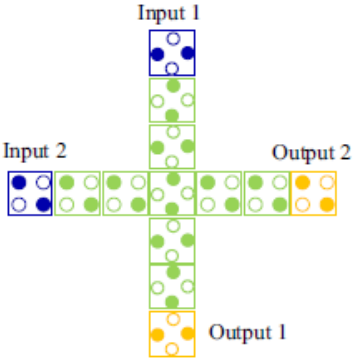
(a)



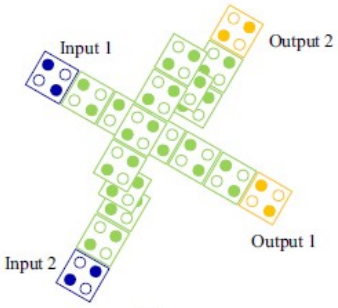
(b)

FIGURE 8. QCA wire (a) wire (90 degree), (b) wire (45 degree).

In the single layer the intersection of two wires is shown in Fig9a. on the other hand, in the multilayer mode the wires are not contact with one another so the data is moved through "via" layer that serves as a bridge as shown in Fig9b [24].



(a)

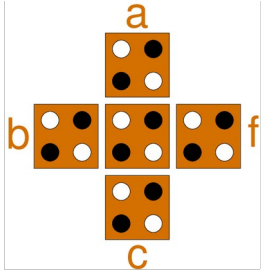


(b)

FIGURE 9. Crossover options: (a) Coplanar crossing, (b) Multi-layer crossing.

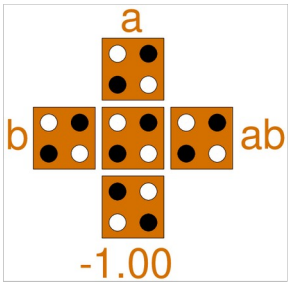
C. QCA MAJORITY GATE AND INVERTER

Majority Voting (MV) gate is a main three-inputs QCA gate that consists of five cells of QCA presented as follows: one cell device, one cell for output, and three cells for inputs as shown in Fig10a [11]. The main formula for MV gate is denoted by the equation: $M(a, b, c) = ab+bc+ac$, where a, b, c are the inputs. The MV gate can works as OR gate in case of assigning one of the MV gate inputs to positive polarization (binary logic "1") as presented in Fig10b, on the other hand it can works as AND gate in case of assigning one of the MV gate inputs to negative polarization (binary logic "0") as presented in Fig10c. Inverter is called NOT gate which is another QCA gate. Fig11 represents QCA inverter gate configuration. The QCA inverter gate reverses the input because the cells are not aligned together which cause different polarization between them [30]. The architecture of NAND gate is presented in Fig12 where the AND gate is utilized before the NOT gate.



(a)

(b)



(c)

FIGURE 10. Using MV gate to construct logic gates: (a) MV gate, (b) OR gate, and (c) AND gate.

FIGURE 11. QCA inverters.

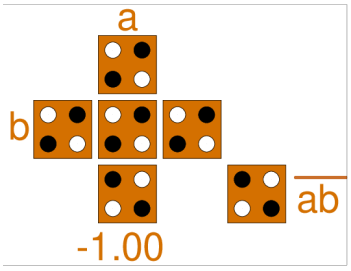


FIGURE 12. QCA

D. QCA CLOCKING

The clocking of QCA is achieved by measuring capacity barriers to the connected quantum-dots. Increasing or decreasing the potential obstruction will allow

full localization control for the free electrons polarization as follows: potential increasing drives components for localization and therefore definite polarization occurs, while decreasing potential allows electrons to be delocalized and no definite cell polarization occurs. For the cells to have equivalent effect of electric field and achieving valid clocking scheme, the cells must be gathered in four stages. There are four stages for clocking in QCA as shown in Fig13. The first stage is the switch stage, the dots barrier is gradually formed to put the electrons to the corners so that the cell is at final polarization of the adjacent cell. The second stage is the hold stage, during this stage the cell is still in polarization and affects the adjacent cells during the increase of the barriers. The third stage is the release stage, at this stage the electrons move to the middle dots because the barriers are decreased causing the cells to lose polarization. The fourth stage is the relax stage where the electrons move to the middle dots making the cell has no definite polarization. The zones should be calculated in certain limits and the form of these zones may be irregular [24]. The proficiency of the QCA designs depend on the exact arrangement the above mentioned zones.

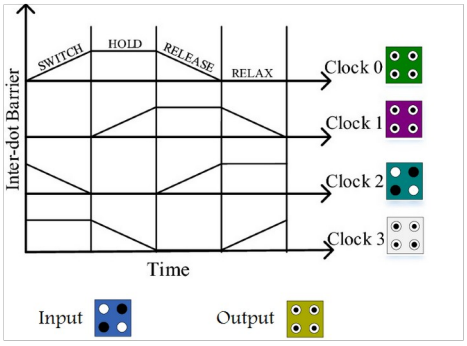


FIGURE 13. **The four phases of the QCA clocking.**

E. LAYOUT DESIGN RULES

Design rules are a collection of parameters in CMOS that help a designer to check the mask set correction. To ensure that circuit components operate properly, a design rule defines some geometric and connectivity constraints. The following are some layout design rules for QCA based on this concept:

1) Single Clocking Zone with Maximum Number of Cells: The physical array is relaxed to its ground state for QCA computation. Temperature sensitivity will make undesired computation with the ground state. More errors will occur due to more cells in same clock zone. Equation 4 shows the limitation on the number of QCA cells to prevent undesired kink.

$$N \leq \frac{E_k}{e^{kB}T} \quad (4)$$

Where N is the number of cells in the array, k_B is the Boltzmann constant, T is the operating temperature, and Kink energy (denoted as E_k). The size of QCA cell has an effect on the overall operating temperature. Higher temperature operation is possible and the size of the cell is decrease because the energy separations between states increase [25]. Operating speed is decreased due to the long wire of QCA that cause increased switching delays and signal propagation. As a result, to ensure proper functionality, the long QCA wires must be divided into separate clocking zones. Since the constraint is dependent on future fabrication technology, it can currently be used as a design parameter.

2) Single Clocking Zone with Minimum Number of Cells: Just one QCA cell can be found in a clocking zone. However, a one-cell clocking zone's waveform can become skewed, and cascading this type of clocking zone can give incorrect results. It is recommended that clocking zones contain at least two cells in a circuit. To prevent the effects of a single-cell clocking zone and ensure robust signal transmission over a long QCA wire, the cells should be divided into different clocking zones [26].

3) Option of Crossover: It is possible to implement crossover in QCA layout by using only one layer called coplanar crossing as shown in Fig9a where both 45 degree and 90 degree cells are used in coplanar crossing. When the two types of cells are correctly aligned, they do not interfere with one another. Although there is failure due to their low robustness and fabrication issues. Another choice is multi-layer crossing, which uses several layers of cells in a manner close to how metal wires are routed in CMOS technology as shown in Fig9b. The extra layers of QCA are thought to be useful as active circuit components and take less space than coplanar circuits. To achieve a robust simulation result in QCADesigner, the most widely used QCA simulator, multi-layer crossing is used. On the other hand, Multi-layer crossovers are difficult to be created. As a consequence, the issue of crossover remains unanswered. The correct response depends on future fabrication technology [27][28].

5) Rules of Timing Design: Proper clocking zone leads to correct QCA layout. Therefore timing rules are important layout in QCA design rules. To ensure equal voting, the timing limitation on a QCA majority gate is that all three inputs must arrive at the device cell at the same time. The device cell will be in the same clocking zone as the inputs if all three inputs wires are the same length. In reality, however, input wire lengths are normally different. So, the majority gate and these three inputs should be constructed with the same clocking zone *i* [29].

IV. PROPOSED QCA FOR REVERSIBLE LOGIC GATES

Reversible gates are combined to synthesize reversible circuits since reversible gates give a bijection mapping between the vector of inputs and the vector of outputs. In this section, QCA designs for CNOT, double CNOT, TOFFOLI, double TOFFOLI, and SWAP circuit will be proposed. In this paper, the version 2.0.3 of QCADesigner is software used for outlining and implementing QCA proposed designs with cohesive simulation engine framework [31]. The proposed designs will be compared with related designs in literature in terms of cell count, area used in the construction, number of majority gate, wire crossover, and clock cycle delay [21] [15]. The parameters which are used in simulation of the proposed QCA designs are shown in Table I. All the proposed designs follow the QCA layout designs rules in terms of all the inputs cells should be arrive in the same time clock zone, long QCA wires should be partitioned in to different clock zone taken in to the considerations of the maximum number of cells and minimum number of cells in the same zone to avoid increased signal propagation and switching delays, and all the proposed designs do not have crossover options.

TABLE I
PARAMETERS USED IN SIMULATION OF PROPOSED QCA CIRCUIT

Temperature	1.000000
Cell Width (nm)	18.000000
Cell Height (nm)	18.000000
Relaxation Time	$1.000000\times10^{-15}10^{-15}$
Time Step	$1.000000\times10^{-16}10^{-16}$
Total Simulation Time	7.000000×10^{-11}
Clock High	9.800000×10^{-22}
Clock Low	$3.800000\times10^{-23}10^{-23}$
Clock Shift	0.000000
Clock Amplitude Factor	2.000000
Radius of Effect	80.000000
Relative Permittivity	12.900000
Layer Separation	11.500000

A. THE PROPOSED DESIGN OF CNOT GATE

Equation 5 shows the functionality of CNOT gate where the inputs can be denoted as *X*, *Y* and the outputs can be denoted as *A*, *B*. The CNOT gate truth table is shown in Table II and the CNOT gate representation is shown in Fig14.

$$A=X\oplus Y \quad (5)$$

$$B=Y$$

An XOR gate implements an Exclusive OR logical operation on two inputs and is denoted by ⊕. The condition of XOR gate to be true is that only one of the inputs is true. When both inputs are false, or both are true, the output result is false. Fig15a represents the suggested QCA design for the CNOT gate. The suggested design consists of a group of 11 cells and there is no clock delay. The simulation results of QCA CNOT gate are shown in Fig15b. The comparison of the suggested CNOT gate with other designs is presented in Table III. Table IV shows the double CNOT gate truth table that represents the CNOT gate reversibility for the proposed design, and Fig16 shows the reversible representation of double CNOT gate. Fig17a represents the suggested QCA design for the double CNOT gate. The suggested design consists of a group of 29 cells and 2 delay of clock cycle. The simulation results of QCA double CNOT gate are shown in Fig17b. The comparison of suggested double CNOT gate with other designs is presented in Table V.

TABLE II
TRUTH TABLE OF 2-INPUT CNOT GATE

X	Y	A	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	1

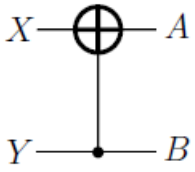
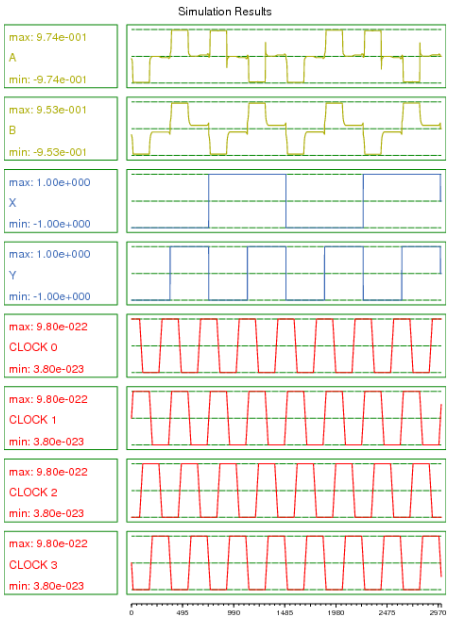


FIGURE 14. CNOT reversible circuit representation.

(a)



(b)

FIGURE 15. CNOT gate: (a) The proposed QCA design, (b) The simulation results.

TABLE III
COMPARING THE SUGGESTED QCA CNOT GATE WITH OTHER PREVIOUS DESIGNS

CNOT gate	Cell Count	Cell Area (nm2)	Delay	No. of MV	Wire Crossover

					gate	
Other designs	Figure 5a in [13]	58	15,660	1.5	4	Coplanar
	Figure 2b in [16]	43	13,932	0.75	3	Coplanar
	Figure 1a in [14]	14	4,536	0	0	Coplanar
	Figure 9b in [15]	23	7,452	0.5	2	Not Required
	Figure 3b in [17]	11	3,564	0.5	0	Coplanar
The proposed design	Fig15	11	3,564	0	0	None

TABLE IV
TRUTH TABLE OF 2-INPUT DOUBLE CNOT GATE

X	Y	A	B
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

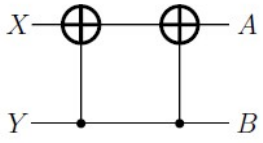
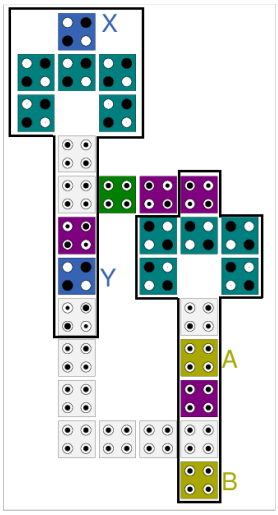
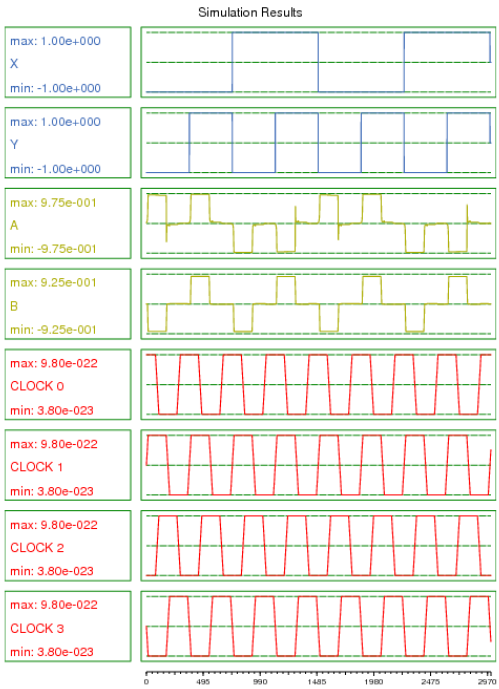


FIGURE 16. **Double CNOT reversible circuit representation.**



(a)



(b)

FIGURE 17. **Double CNOT gate: (a) The proposed QCA design, (b) The simulation results.**

TABLE V
COMPARING THE SUGGESTED QCA DOUBLE CNOT GATE WITH OTHER PREVIOUS DESIGNS

Double CNOT gate		Cell Count	Cell Area (nm2)	Delay	No. of MV gate	Wire Crossover
Other designs	Figure 9b in [18]	51	16,524	0.5	6	Coplanar
	Figure 18 in [19]	93	30,132	0.75	6	Coplanar
	Figure 10b in [15]	40	12,960	4	4	Coplanar
The proposed design	Fig17	29	9,396	2	0	None

B. THE PROPOSED DESIGN OF TOFFOLI GATE

Tommaso Toffoli proposed a universal reversible gate called TOFFOLI gate [32] which can be used to build the reversible version of

any classical gate. Equation 6 describes the functionality of TOFFOLI gate where the inputs can be denoted as *X, Y, Z* and the outputs can be denoted as *A, B, C*. TOFFOLI gate negates first input if the second and the third control inputs are set to binary logic "1" otherwise the first input stays unchanged [32]. The TOFFOLI gate truth table is shown in Table VI and Fig18 shows the reversible representation of TOFFOLI gate. Fig19a represents the suggested QCA for TOFFOLI gate. The suggested design consists of 10 cells with one delay of clock cycle, and the results of simulation are presented in Fig19b. The comparison of suggested TOFFOLI gate with other designs is presented in Table VII. Table VIII shows the double TOFFOLI gate truth table that represents the TOFFOLI gate reversibility for the proposed design, and the representation of the reversible gate is shown in Fig20. The proposed double TOFFOLI gate consists of 44 cells with 5 delay of clock cycle as shown in Fig21a and the simulation results are shown in Fig21b.

$$A=X\oplus YZ \quad (6)$$

$$B=Y$$

$$C=Z$$

TABLE VI
TRUTH TABLE OF 3-INPUT TOFFOLI GATE

X	Y	Z	A	B	C
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	1	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	0	1	1

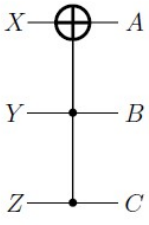
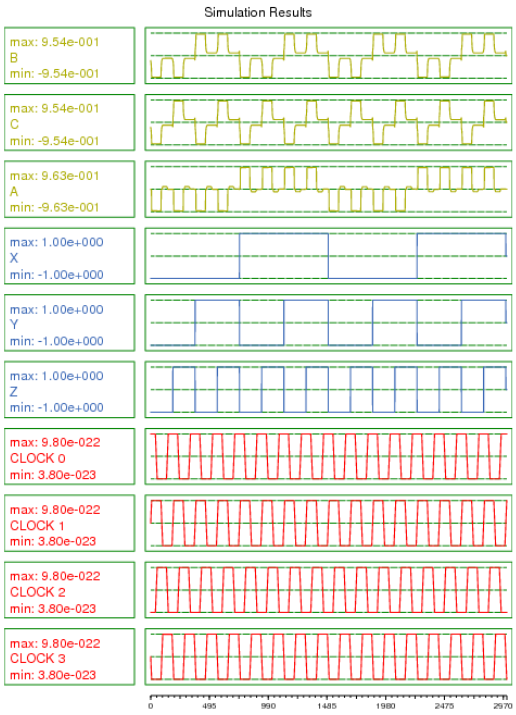


FIGURE 18. TOFFOLI reversible

(a)



(b)

FIGURE 19. TOFFOLI gate: (a) The proposed QCA design, (b) The simulation results.

TABLE vII
COMPARING THE SUGGESTED QCA TOFFOLI GATE WITH OTHER PREVIOUS DESIGNS

Toffoli gate		Cell Count	Cell Area (nm2)	Delay	No. of MV gate	Wire Crossover
Other designs	Figure 7a in [13]	64	20,736	1.5	5	Coplanar
	Figure 4 in [20]	24	7,776	0.5	2	Coplanar
	Figure 6 in [21]	33	10,692	0.75	1	Multilayer
	Figure 12 in [22]	45	14,580	0.75	3	Not Required
	Figure 1b in [14]	20	6,480	2	2	Coplanar
	Figure 11b in [15]	34	11,016	0.75	3	Multilayer
The proposed design	Fig19	10	3,240	1	0	None

TABLE VIII
TRUTH TABLE OF 3-INPUT DOUBLE TOFFOLI GATE

X	Y	Z	A	B	C
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	1

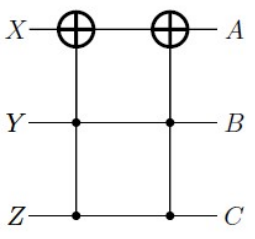
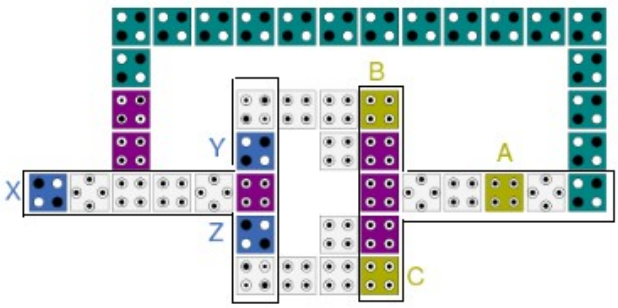
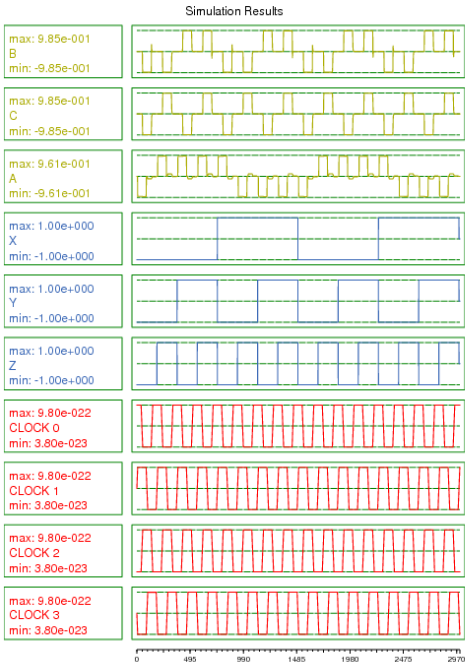


FIGURE 20. Double TOFFOLI reversible circuit representation.



(a)



(b)

FIGURE 21. Double TOFFOLI gate: (a) The proposed QCA design, (b) The simulation results.

C. QCA FOR REVERSIBLE CIRCUITS

In this section, the proposed CNOT gate design will be used for building a design for the QCA SWAP reversible circuit. The proposed TOFFOLI gate design will be used for building a QCA reversible circuit design that consists of combination between five NOT gates and one TOFFOLI gate. SWAP circuit consists of a combination of 3 CNOT gates, and it exchanges the inputs. Table IX shows the truth table of SWAP circuit and Fig22 shows the SWAP circuit representation. The proposed SWAP circuit design consists of 55 cells but with 2 clock cycles delay as shown in Fig23a and the simulation results are shown in Fig23b. Comparing other QCA designs for the SWAP circuit with the proposed design is shown in Table X.

TABLE IX
TRUTH TABLE OF SWAP CIRCUIT

X	Y	A	B
0	0	0	0
0	1	1	0
1	0	0	1
1	1	1	1

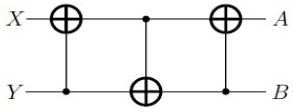
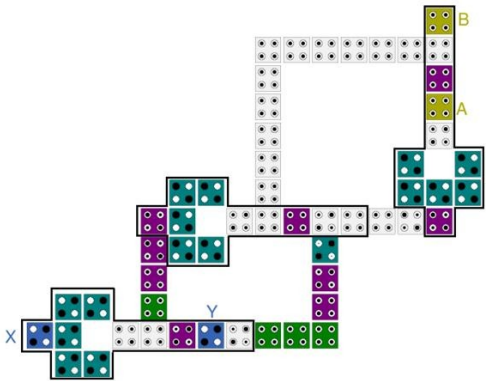
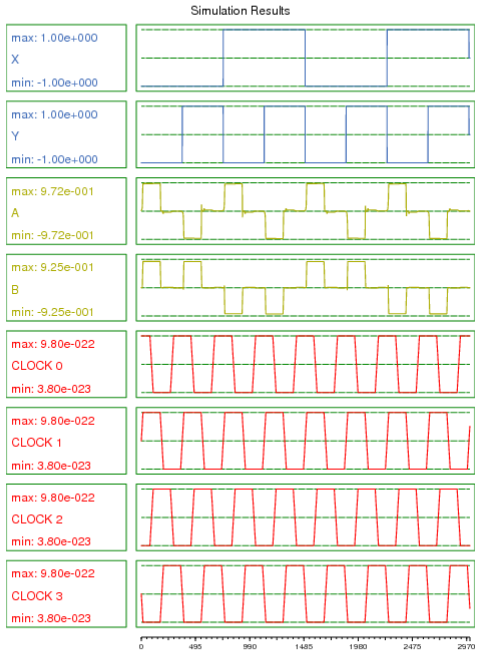


FIGURE 22. The reversible circuit representation for the SWAP circuit.

(a)





(b)

FIGURE 23. SWAP circuit: (a) The proposed QCA design, (b) The simulation results.

TABLE X
COMPARING THE SUGGESTED QCA SWAP CIRCUIT WITH OTHER PREVIOUS DESIGNS

SWAP circuit		Cell Count	Cell Area (nm2)	Delay	No. of MV gate	Wire Crossover
Other design	Figure 17 in [23]	1730	560,520	9	27	Multilayer
	Figure 4h in	135	43,740	2.75	0	Multilayer

s	[21]					
The proposed design	Fig23	55	17,820	2	0	None

Another design of QCA will be proposed for a reversible circuit. A reversible circuit is constructed using single TOFFOLI gate together with five gates of inverter gate as shown in Fig24 and Table XI shows the reversible circuit truth table. The proposed reversible circuit contains 12 cells with 3 delay of clock cycles as shown in Fig25a and the simulation results are shown in Fig25b.

TABLE XI
TRUTH TABLE OF THE REVERSIBLE CIRCUIT WITH SINGLE TOFFOLI AND FIVE NOT GATES

X	Y	Z	A	B	C
0	0	0	0	0	0
0	0	1	1	0	1
0	1	0	1	1	0
0	1	1	1	1	1
1	0	0	1	0	0
1	0	1	0	0	1
1	1	0	0	1	0
1	1	1	0	1	1

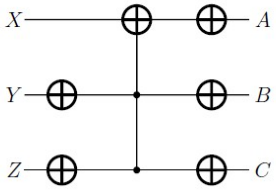
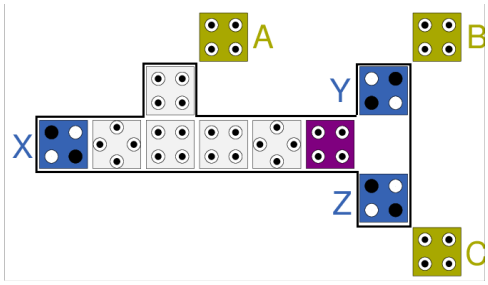
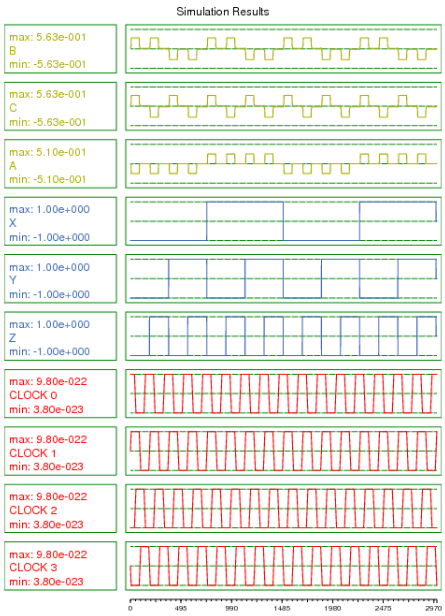


FIGURE 24. Reversible circuit with single TOFFOLI and five NOT gates representation.



(a)



(b)

FIGURE 25. Reversible circuit with single TOFFOLI and five NOT gates representation.

V. CONCLUSION

This paper proposed novel QCA designs for the CNOT and TOFFOLI gates. The proposed QCA design for the CNOT gate has been used to design QCA for the double CNOT gate to verify its reversibility and is also used to design QCA for the SWAP circuit that contains a combination of three CNOT gates. The proposed QCA for the CNOT and TOFFOLI gates has been used to design the QCA for the circuits by adding cells with certain clocks to the wires that connects the proposed gates. The proposed QCA design for the TOFFOLI gate has been used to design QCA for the double TOFFOLI gate, and is also used to design QCA for a reversible circuit with one TOFFOLI and five NOT gates to show the efficiency of the proposed designs. The proposed QCA designs are compared with related designs proposed by others. The comparisons show that the

proposed designs are better in terms of the number of cells used, the area occupied, the number of MV gates, the layers of construction, and/or the clock cycle delay, which reflects that the proposed designs are more efficient than other designs. The presence of smaller faults in QCA design lead to more errors about its interactions. The best way to avoid such errors is to design the QCA circuit logic which provides performance in the presence of some errors. These designs allow some defects to be cancelled out by other cells which are in correct state. An extension to the work in this paper is to use an extended version of all the proposed designs to work for faults and generate reversible gates that give the correct output in the presence of faults.

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